

Thermal-Aware Modeling of Physical Unclonable Functions for Reliable Hardware Security in 3D Integrated Circuits

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Abstract

Three-dimensional integrated circuits (3D ICs) are intended to achieve high integration density and short vertical interconnections, however, with the stacking of active layers, power density, thermal gradient, and reliability sensitivity increase. Physical unclonable functions (PUFs) are appealing choices for hardware-security primitives, as they rely on manufacturing variations that are not controllable to produce a device-specific response. The delays and device variations of the process, however, are also temperature sensitive, which is the source of the PUF entropy. In this paper, a thermal-aware modeling framework for PUFs embedded in 3D ICs based on TSV is developed. It integrates a vertically stacked thermal model with a temperature dependent PUF response model, allowing local temperature, TSV proximity and process variations to be simultaneously taken into account for reliability evaluation. Ring-oscillators and Arbiter-type PUFs are considered representative structures and the variation caused by TSV is considered as an extra entropy source. The evaluation method is based on the main evaluation metrics: reliability, uniqueness, uniformity, bit-error rate, intra-chip Hamming distance, and thermal sensitivity. Existing 3D-IC PUF research shows that process variation from CMOS, TSV, can both introduce entropy, and recent reliability studies demonstrate that temperature and voltage variation can have a significant impact on PUF stability. The proposed framework is a systematic approach to the thermal-aware placement of PUFs, modelling of their responses, and optimization for reliability in a stacked hardware-security architecture.

Keywords—3D IC, physical unclonable function, thermal-aware modeling, TSV, hardware security, temperature variation, reliability.

I. Introduction

Due to the shift from planar scaling to heterogeneous and vertically integrated systems, the interest in 3D ICs has grown. 3D integration can decrease the length of the interconnect and increase the integration density by stacking each active die and electrically connecting them using through-silicon vias (TSVs). Concurrently, the vertical stacking reduces the heat removing paths and can produce high temperature differences between tiers. The thermal management challenges have been reported as a critical issue for TSV based 3D ICs; due to heat generated by one layer, it can be transferred to the adjacent active layer, which is not the cooling boundary [8, 9].

The individual die, TSV, interposers and package interfaces provide new attack surfaces, making hardware security more critical than ever. PUFs are a small hardware primitive that are based on the principle of mapping the differences in manufacturing components to the resulting fingerprints on the device. The most important features are uniqueness across devices and reliability of a given device across different environments and operating conditions [15].

The central issue presented here is that the physical origin of PUF entropy and the circuit path on which PUF entropy is observed are both temperature dependent. In the case of delay-based PUFs, the temperature affecting the transistors has an impact on their mobility, threshold voltage, interconnect resistance and propagation delay. In a 3D stack, these effects are nonuniform across space, so that two PUFs with seemingly identical designs may be subjected to varying temperatures in different tiers, at different power neighborhoods, due to different TSV densities and/or distances from the heat-removal path.

A published 3D-IC PUF architecture used process variability of both CMOS devices and TSVs. This reported 6-layer 3D IC structure and HSPICE simulation of 100 PUF chips demonstrated that TSV variation can be employed to provide another source of uniqueness [1].

Contributions

(1) Coupled thermal-PUF modeling framework for TSV based 3D ICs;

- (2) a temperature dependent delay model of ring oscillator and arbiter PUFs;
- (3) a BER- and Hamming-distance-aware reliability methodology; and
- (4) Design guidance for placement of PUF and entropy extraction that is aware of TSV.

II. Background and Related Work

A. PUF Fundamentals

A PUF is based on physical changes which are not easily reproduced. For challenge C, a PUF generates a response R which varies according to the physical properties of a specific integrated circuit. A delay-based implementation involves comparing two identical paths made up of slightly different components, where the component in one path is made faster than that in the other. A stable PUF is able to preserve this ordering in repeated evaluations with different response distributions over different devices.

The reliability, uniqueness, uniformity and bit-aliasing are important metrics. Reliability is often computed as the percentage of the response bits that do not change if the same device is tested under different conditions. Uniqueness measures the distance between the devices, and uniformity measures the uniformity of the zeros and ones. These parameters should be considered within a temperature field instead of at one ambient temperature for a thermal-aware 3D design.

B. PUFs in 3D Integrated Circuits

The integration space of 3D designs is altered by the fact that TSVs serve as both electrical connectors, structures and thermal paths. The 3D-IC PUF architecture in [1] explicitly made use of process variation in the CMOS devices and TSVs. This means that vertical integration can be a part of the entropy-generation process.

Local thermal and geometric nonuniformity is also introduced by the TSV. The TSVs are filled with copper, which can alter the local heat flow, and the interfaces and the dielectric around the TSV can add thermal resistance. However, recent thermal reviews have indicated that dimensions of TSV, TSV pitches, filling material, interfaces, and TSV layouts can have an impact on temperature distributions and reliability [8]–[11].

C. Temperature Sensitivity of PUFs

One of the common reliability issues in delay-based PUFs is the temperature sensitivity. The experimental analysis results indicate that the supply-voltage and temperature variations can also affect PUF-reliability as much as other variation sources [2]. Recently studied circuits are thus those that are temperature-invariant. In recent years, current-starved-inverter PUFs are reported with better reliability in the temperature range of -40°C to 120°C , and another reliability-aware PUF study evaluated bit flips within the range of -20°C to 80°C [3], [5]. The studies give reasons for a specific temperature model, rather than consider temperature as a nuisance variable.

D. Research Gap

The current research is mostly focused on either PUF circuits that are tolerant to temperature or thermal models for 3D IC structures. There is a smaller body of work that directly connects the two. The gap is especially significant for stacked PUFs where temperature is spatially distributed and correlated with the location of the TSVs and neighboring activities. The thermal-aware PUF model should thus be able to represent temperature propagation through the 3D physical stack and further propagate it to delay and security metrics.

III. Proposed Thermal-Aware Puf Model

The proposed framework has four phases: 3D physical and power modelling, generation of the thermal-field, modelling of the PUF response as a function of temperature, and statistical security evaluation. The thermal solver outputs $T(x,y,z,t)$ which is assigned to each element of the PUF. Then, process variation, variation due to TSV, and variation due to thermal delay are combined to yield responses for various operating conditions.

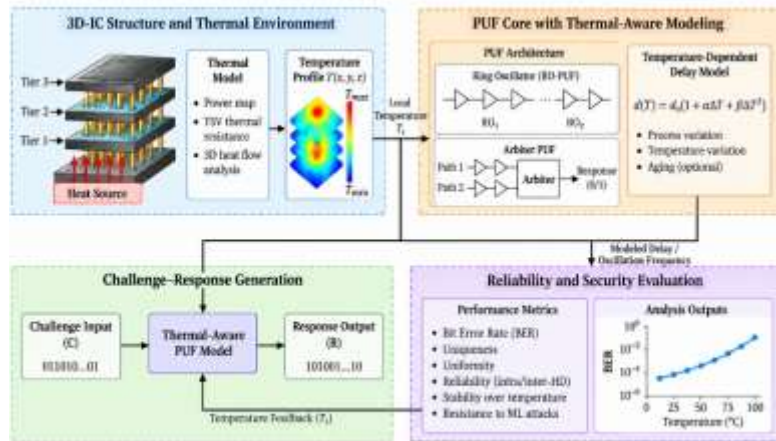


Fig. 1. Thermal-aware PUF model for reliable hardware security in 3D integrated circuits.

IV. Thermal Modeling of the 3d Puf Environment

A. Layered Thermal Representation

The transient heat conduction in a homogeneous region can be written as $\rho c(\partial T/\partial t) = \nabla \cdot (k \nabla T) + Q$, where Q is heat generation; c is specific heat; k is thermal conductivity; and ρ is density. A small RC network can discretize active silicon, dielectric, TSV regions, bonding layers, heat spreader and package boundaries. The intent is to create a local temp for each PUF element.

A compact model is helpful because the multiscale thermal simulation of modern 3D ICs is still challenging because of interface effects, material anisotropy and significant spatial scale differences [9]. The framework can thus be applied initially to an RC model and subsequently compared to a FE solution.

B. TSV and Hotspot Effects

The thermal field is influenced by the material, the geometry and the location of the TSVs. Their size and pitch change vertical heat conduction and their electrical function is correlated with power and routing density. The thermal studies have demonstrated that the geometric, pitch, aspect ratio and stacking configuration of TSV can influence the junction temperature and thermal resistance [10-11].

Two PUFs in close proximity to a high power block may have different power temperature characteristics than two PUFs near a heat removal path. The model thus attributes a local temperature offset ΔT to each PUF, instead of having a single temperature value.

C. Temperature-Dependent Delay Model

In a delay based PUF, propagation delay of element is used. For large temperature excursions, a first order expression should be replaced by SPICE derived lookup tables or nonlinear compact models.

D. Ring-Oscillator PUF

RO PUF is a comparison of the oscillation behavior of two nominally identical oscillators. The thermal-aware model is designed to use the local temperature for each oscillator to assess the performance of that oscillator. A response changes when the thermal induced differential delay approaches the process induced delay margin. Therefore, the reliability is not only a function of absolute temperature, but also of the difference between the absolute temperature of the oscillators.

E. Arbiter PUF

A configurable delay stage is used in the arbiter PUF to propagate a transition through two paths. The arbiter writes the name of the path that gets there first. Each stage has a local temperature with which to associate the

total path delay will be affected by temperature gradients. This is more representative of a 3D stack than of having one temperature for the whole circuit.

F. TSV Variation as an Entropy Source

TSV dimensions, resistance, capacitance, and local process deviations can be included in $\Delta d_{TSV,i}$. This follows the 3D-IC PUF concept demonstrated in [1], where TSV variation was intentionally used as an additional physical source of variation.

V. Thermal-Aware Reliability Evaluation

A. Evaluation Procedure

The evaluation starts with a reference 3D stack and instances of PUFs across tiers. A statistical distribution is used for the assignment of process parameters. The thermal model is solved for a variety of operating conditions, and the local temperature is passed to the PUF delay model. This is repeated on different devices and repeated measures to estimate intra- and inter-device behavior.

The practical workflow is: create the 3D stack; extract the layer-wise power maps; solve the thermal field; map the elements of the PUF to the local temperature; extract the delays depending on the temperature; generate responses; calculate reliability, uniqueness, uniformity, BER, and Hamming-distance metrics.

B. Reliability and BER

The normalized Hamming distance between R_{ref} and R_T can be used to estimate the thermal BER. The reliability is $1 - \text{error rate}$. This directly relates the temperature-dependent response instability to a security metric.

C. Intra-Chip and Inter-Chip Hamming Distance

Intra-chip Hamming distance measures response variations for the same device when subjected to a change of temperature or voltage. Good reliability is reflected in a low intra-chip distance. Inter-chip Hamming distance is used to measure the difference between the responses of the various devices and should be close to the ideal mid-point for good uniqueness. Dispersion as well as mean should be included.

D. Uniformity and Bit Balance

The uniformity is the proportion of response bits that are all a single value. If one set of delay paths is maintained at a different temperature, this will result in systematic shifts (thermal bias). Thermal-aware evaluation should thus verify that gradients cause bit imbalance as well as bit flips.

E. Proposed Evaluation Matrix

Factor	Suggested range	Output
Temperature	25–100 °C	BER / reliability
Local gradient	0–30 °C	Thermal sensitivity
Supply voltage	±10% nominal	PVT robustness
Process variation	Monte Carlo	Uniqueness
PUF location	Tier 1–Tier 6	Placement sensitivity
TSV proximity	Near / medium / far	TSV effect

The ranges listed above are design-study conditions, not measured results. Refinement for the selected technology node, PUF architecture, stack, and cooling boundary should be performed on them at the final circuit level.

VI. Model-Based Analysis

The coupled model predicts three dominant behaviors. First, as the thermal-induced differential delay gets close to the delay margin due to the processing, the reliability drops. Second, PUFs in warmer levels or closer to power hotspots are more thermally sensitive. Thirdly, adding more thermally coupled active layers can widen the temperature distribution range and introduce variance to the response. These trends are consistent with known

thermal 3DIC reliability challenges from the thermal literature including high power density, limited heat removal, and layer-to-layer heat interaction [8] [9] [13].

VII. Thermal-Robustness Strategies

Ideally, a thermally robust PUF would be one that maximises separation between competing paths created by the process, and minimises the difference in thermal sensitivity between them. Some useful approaches are symmetric placement of competing paths, thermal-aware floorplanning, calibration of temperature-sensitive cells, differential sensing, and choosing PUF instances that have adequate nominal delay margin.

For 3D stacks, a PUF may be spread across several different components (hotspots), which makes it possible to prevent any single component from dominating a security primitive. Thermal TSVs and heat-spreading structures can help to mitigate hotspots, but they must be co-optimized with signal TSVs since they are competing for physical space [14].

VIII. Security and Reliability Discussion

A. Security Implications of Thermal Variation

There are two security implications on thermal variation. The first is reliability: A valid device can respond differently when heated in a different manner. The second is the potential for the leakage of information: If the response changes regularly as a function of temperature, an attacker who can control or observe the temperature can obtain information from the delay structure. The systematic response bias should, therefore, be assessed in a thermally-aware PUF as well as the average reliability.

This is especially applicable to a 3D system as it is because heat can be used to detect activity in adjacent tiers. Many PUFs near a high-power accelerator might have a workload-dependent temperature signature. If this signature impacts the response, then the security primitive might be workload dependent.

B. Modeling Attacks and CRP Behavior

Strong PUFs reveal numerous challenge-response pairs, and can be susceptible to mathematical modeling attacks if the challenge function has too much regularity. Another physical variable is added by thermal variation. It can either make things more complicated or provide new structure to exploit by an attacker if unregulated. The thermal-aware design should then be defined by temperature sensitivity, rather than by temperature. Thermal-aware design should therefore be defined by temperature sensitivity, not by temperature.

In recent PUF studies, more and more, reliability enhancement is accompanied by machine-learning attack resistance. Recently, a temperature-invariant RO-PUF-based scheme was presented that achieved better reliability over a broad temperature range, but also reduced the accuracy of ML attacks, demonstrating the need to consider environmental robustness and attack resilience simultaneously [5].

C. Comparison With Existing Studies

Approach	Temperature condition	Main observation
3D-IC TSV PUF	Process-variation simulation	TSV variation used as entropy
SDC PUF	25–75 °C + VT	Improved reliability
ZTC/CS PUF	–40–120 °C	Temperature robustness
Current-mirror PUF	–20–80 °C	Temperature-dependent stability
Proposed model	Technology dependent	Local thermal map → response

These are not reproduced experiments of this paper [1]–[5], but instead are a summary of published studies that position the proposed framework in the first four rows.

D. Thermal-Aware PUF Placement

Placement is one of the key variables of 3D Design. One of the easiest approaches is to not have competing delay paths on vastly contrasting thermal regions. A better approach is to "co-locate" both paths in a similar thermal environment with retaining the necessary process variation. Oscillator pairs for RO PUFs need to have similar thermal history, while competing paths for arbiter PUFs need to be sensitive to similar regions.

A combined score, which includes the nominal delay separation, thermal coefficient, BER under temperature variations, area and power, can be used to rank candidate PUF instances. Only occurrences with the necessary reliability level are kept for key generation.

E. Limitations

This paper is based on a modeling framework, not fabricated-silicon measurements. The design-study temperatures given are only proposals and should not be taken as actual performance. The actual response will vary according to technology node, transistor models, TSV geometry, materials, cooling boundary condition, supply voltage and PUF implementation.

Another drawback is electrothermal coupling. Assuming that the power is known regardless of temperature, the thermal model is decoupled, but the leakage and switching power may vary as a function of temperature. Future work should be repeated until the electrical and thermal fields converge, starting with an initial electrical power estimation and then running a thermal analysis.

IX. Practical Implementation Flow

The implementation can be divided into six stages: (1) 3D stack and material definition; (2) acquisition of power maps at every layer; (3) solving the thermal field; (4) mapping local temperature to the PUF elements, and computing the temperature-dependent power delay; (5) computing responses to process and environment variations; and (6) computing reliability, uniqueness, uniformity, BER, Hamming distance and security metrics.

X. Design Recommendations and Conclusion

A. Design Recommendations

According to the thermal-aware model, the ratio of process-induced delay difference to thermal-induced differential delay determines the reliability of PUF. The response is stable if the nominal path difference is large compared with the thermal perturbation. Once the two quantities are approximately equal, even a small temperature difference will lead to a response inversion. Thus, the pairs selected for candidates should have enough delay margin compared to its temperature coefficient.

When planning security-block floorplanning, tier selection must be taken into account as well. While the coolest tier may be optimal, there is no guarantee that it is the optimum tier, because it is also the tier that offers the necessary physical variation while maintaining the necessary thermal environment. Therefore, thermal maps are recommended to be taken into consideration prior to final placement of PUFs.

The physical environment should be modeled as TSVs. They can control thermal conduction, parasitics, stress, and process variation. The previous 3D-IC PUF publications have revealed that intentional TSV variability can be incorporated into the system to increase entropy [1]. The proposed framework takes this a step further and incorporates the thermal field of the TSV-aware stack.

B. Recommended Conference Evaluation

Evaluation	Conventional	Thermal-aware
Response	Nominal temperature	Local $T(x,y,z)$
Reliability	Repeated nominal tests	Temperature sweep
Uniqueness	Inter-device HD	HD across thermal states
TSV impact	Electrical variation	Electrical + thermal
Placement	Area/routing	Area + hotspot map
Security	CRP statistics	CRP + thermal leakage

This assessment directly tackles a problem with traditional PUF assessment in 3D ICs: the response is treated as a purely electrical fingerprint despite the physical environment being 3-dimensional and thermally nonuniform.

C. Conclusion

The presented paper introduced a thermal-aware modeling framework for PUF based reliable hardware security in 3D integrated circuits. The main concept is to consider the temperature as a space varying physical property, which directly impacts the delay elements, which produce the PUF responses. The framework integrates a 3D thermal model, the physical variation aware of TSV, circuit delay variation with temperature, and statistical PUF evaluation. It can be used for the ring-oscillator, arbiter, and other delay-based PUF architectures.

The following two points from the literature are important to note: 3D-IC PUFs are able to take advantage of the process variation of CMOS devices and TSVs, and temperature and voltage variation can significantly affect the reliability of PUFs [1] [2]. These effects are combined with layer specific thermal gradients and hotspot behavior in a stacked architecture, and thermal-aware evaluation is necessary.

The suggested approach is hierarchical in the following way: 1) the 3D temperature field is derived; 2) the temperature field is mapped to the PUF elements; 3) the response is generated and the reliability is computed. Process Variation is crucial for PUF uniqueness but can be enhanced by Thermal-aware placement, Symmetric path environments, Adequate delay margin, and TSV-aware modeling, with the result of maintaining robustness without discarding the process variation. Future work could involve the framework being implemented using a technology calibrated 3D thermal solver and transistor level Monte Carlo simulation and then verified on silicon or hardware.

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